from gate **101**. Connection is made to the gate at some suitable edge portion of the wafer.

FIGS. **9** and **10** show the shape of measured curves which demonstrate the reduction in forward resistance when the region **40** is made highly conductive (n+). In FIG. **9**, the device tested had a region **40** which had the n(−) resistivity of the epitaxial region. Thus, the forward resistance is characteristically high at different gate biases as shown in FIG. **9**.

In the device of the invention where region **40** is of n(+) conductivity, there is a dramatic decrease in the on-resistance as shogun in FIG. **10** for all gate voltages before velocity saturation of the electrons occurs.

Although the present invention has been described in connection with a preferred embodiment thereof, many variations and modifications will now become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

What is claimed is:

1. A semiconductor device comprising, in combination: a thin, flat semiconductor wafer, junction isolation means for dividing said semiconductor wafer into at least first and second laterally separated segments; said first segment containing at least one power MOSFET device; said junction isolation means including a P+ sinker diffusion which encloses said first segment; said at least one power MOSFET device in said first segment including at least first and second spaced base regions each having a respective source region which forms a surface channel region within its respective base region extending from said source region to a respective edge of said respective base region, the respective edges each adjoining a common conduction region; and a gate means disposed parallel to said channel regions and operable to invert said channel regions; source electrode means connected to each of said source and base regions and disposed on the top surface of said wafer; and a drain electrode electrically coupled to said common conduction region, and disposed on the top surface of said wafer.

2. The device of claim **1**, wherein said drain electrode is on said top surface of said wafer and is electrically insulated from said source electrode means.

3. The device of claim **1**, wherein said first and second spaced base regions are diffusion regions which extend from the top surface of said wafer; at least one of said base-regions having a closed polygonal topology.

4. The device of claim **3**, wherein said first base region has a first relatively deep portion and a second relatively shallow portion, said relatively shallow portion disposed between said first relatively deep portion and said edge of said first base region.

5. A semiconductor device comprising:

a wafer of semiconductor material having first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped, one conductivity type major body portion;

the area of said wafer being divided into at least first and second spaced electrically isolated segments, said first segment including a power device and said second segment including at least one other device; the power device of said first segment comprising:

at least first and second spaced base regions of the opposite conductivity type to said one conductivity type formed in said first segment and extending from said first surface to a depth beneath said first surface; the space between said at least first and second base regions defining a common conduction region of said one conductivity type at a given first surface location;

first and second source regions of said one conductivity type formed in said at least first and second base regions, respectively, at first and second first surface locations and extending from said first and second first surface locations to a depth less than said depth of said base regions; said first and second source regions being laterally spaced along said first surface from the facing respective edges of said common conduction region thereby to define first and second channel regions along said first surface between said first source region and said common conduction region and between said second source region and said common conduction region, respectively;

source electrode means located on said first surface, connected to said source regions and comprising a first terminal;

gate insulation layer means on said first surface and disposed at least on said first and second channel regions;

gate electrode means on said gate insulation layer means, overlying said first and second channel regions and comprising a second terminal;

a drain conductive region remote from said common conduction region and extending from said first surface into said major body portion; and

a drain electrode located on said first surface, coupled to said drain conductive region and comprising a third terminal whereby a current path is defined between said source electrode means and said drain electrode which has a first vertical component from said source electrode means through said common conductive region, a lateral component beneath said at least first and second spaced base regions and a second vertical component from beneath said at least first and second spaced base regions to said drain electrode.

6. The device of claim **5** wherein said wafer of semiconductor material further includes a laterally extending relatively thin buried drain region disposed within said drain conductive region and being of said one conductivity type and having a concentration greater than the concentration of said relatively lightly doped major body portion, and extending beneath and spaced from said common conduction region and said at least first and second base regions; said buried drain region at serving to reduce resistance to lateral current flow between said common conduction region and said drain conductive region.

7. The device of claim **5**, wherein each of said at least first and second spaced base regions of said opposite conductivity type has a respective profile which includes a relatively shallow depth region extending from said common conduction region and underlying a corresponding one of said first and second source regions and which includes a respective relatively deep, relatively large radius region extending from said relatively shallow depth region and which is laterally spaced from beneath said corresponding source region on the side of said source region that is away from said common conduction region; said relatively large radius region at least partially underlying its said corresponding source region.

8. The device of claim **5**, wherein said common conduction region is relatively highly doped, compared to said relatively lightly doped major body portion and extends from said given first surface location to a depth greater than the depth of said source regions, whereby resistance to current flow at the junctures between said first and second